REMARKS

Claims 28 – 49 are pending in the application.

Claim 43 has been amended to address the Examiner's 35 U.S.C. 112 indefiniteness rejection. Any further suggestions for amending this claim would be welcomed.

The Examiner is thanked for the telephone indication that claims 40 and 43 would be allowable. However, based on the following comments, it is respectfully submitted that all of the pending claims 28 – 49 should be allowable.

The Examiner has rejected independent claim 28 and others as being unpatentable under 35 U.S.C. 103(a) over Kodama. Applicants respectfully submit that such a rejection is not warranted.

In particular, Kodama discloses a method of making a semiconductor device with a shallow PN junction depth on the order of 50 nm. The method of Kodama proceeds from the recognition that after an ion implantation in a substrate, and a subsequent thermal treatment, foreign atoms diffuse into the semiconductor substrate approximately to a depth of 100 nm. If point defects occur in a silicon substrate, then over and above the thermally enhanced diffusion, there furthermore results a diffusion that is enhanced by the defects (defect enhanced diffusion); such defect enhanced diffusion can not be controlled by Kodama without further steps having to be taken.

In order to now provide a flat PN junction depth, Kodama first selectively applies a silicon layer (raised layer) in that region in which a flat PN junction is to be formed; such a silicon layer (raised layer) contains carbon or nitrogen, the purpose of which is to

combine with the point defects and thus prevent a defect enhanced diffusion (see column 4, first paragraph of Kodama).

Pursuant to Kodama, the selectively applied silicon layer (raised layer) has a thickness of 60 nm in order to produce a PN junction depth of 40 nm. As clearly set forth in Kodama, the thickness of the applied silicon layer is directly proportional to the PN junction depth (see column 3, lines 21 – 31).

Thus, in order to achieve a significant reduction of the junction depth, it is necessary to provide a considerable depth for the applied layer (raised layer). This is due to the fact that after the application of the silicon layer, foreign atoms are implanted into the applied layer via ion implantation. During a subsequent thermal treatment of the substrate, the foreign atoms diffuse into the applied layer and into the substrate disposed below the layer, and in particular pursuant to Kodama to a depth of 100 nm from the surface of the applied layer.

Thus, from the foregoing it can be seen that Kodama controls the depth of a PN junction directly via the thickness of the applied silicon layer. However, it is respectfully submitted that Kodama provides no disclosure with regard to the composition of the silicon layer.

In distinct contrast to the teaching of Kodama, independent claim 28 of the instant application provides a method for generating defects in a lattice structure of a semiconductor material during thermal treatment of the material. Defects in the lattice structure include, in particular, so-called vacancies and atoms on interstitial lattice positions. The defects that are produced influence the diffusion characteristics of

fig 2
9.10

foreign atoms within the semiconductor material. Thus, claim 28 of the present invention is directed specifically to the generation of defects in a lattice structure of a semiconductor material in order to achieve a defect enhanced diffusion. Thus, it is respectfully submitted that the present invention is in direct contrast to the subject matter of Kodama, pursuant to which a defect enhanced diffusion is to be prevented (see the aforementioned passage of column 4, and in particular lines 8 and 9). In addition, pursuant to claim 28 of the instant application, a concentration and/or a distribution of defects or vacancies is controlled as a function of a process gas atmosphere. It is respectfully submitted that Kodama neither teaches nor suggests such a control of the concentration and distribution of defects or vacancies as a function of a process gas atmosphere. Kodama merely teaches the selective growth of a silicon layer (raised layer) and provides no teaching concerning a control of a concentration and a distribution of defects or vacancies as a function of a process gas atmosphere.

Finally, pursuant to claim 28 of the instant application, either an $Si_xO_yN_z$ oxy-nitride layer having a thickness of up to 2 nm, or an Si_3N_4 layer having a thickness of up to 4 nm, is applied to the semi-conductor. This layer, among other things, has the function of preventing foreign atoms from diffusing out of the semiconductor material. Due to its slight thickness, such a layer is in no way comparable to the silicon layer (raised layer) that is applied in Kodama. In particular, if layer thicknesses of 2 to 4 nm were to be used in the method of Kodama, this would lead to an entirely insignificant reduction of the PN junction depth, namely to a reduction of 2 to 4 nm.

It is respectfully submitted that this is further evidence that the layer defined in claim 28 of the instant application is clearly in no way comparable to the silicon layer applied pursuant to Kodama, so that the method of claim 28 is clearly distinguishable from any teaching of Kodama.

It is respectfully submitted that the Examiner's assertion, that the slight thickness of 2 to 4 nm is merely an optimization of the layer thickness of Kodama, is incorrect. Rather, the layers of Kodama and those of the present invention as defined in claim 28 have entirely different functions, as explained above. Thus, It is respectfully submitted that claim 28 of the instant application is clearly distinguishable over the Kodama reference.

It is furthermore respectfully submitted that even a combination of Kodama with Wolf would not suggest the subject matter of any of the claims of the instant application, since Wolf also provides no teaching or suggestion to control at least one of a concentration and a distribution of defects or vacancies as a function of a process gas atmosphere, as required by claim 28. Rather, Wolf relates only to the application of various layers upon a semiconductor substrate, and not even upon the specifically mentioned layers of claim 28 with layer thicknesses of 2 or 4 nm, which have the aforementioned functions.

In view of the foregoing discussion, Applicants respectfully request reconsideration of the allowability of all of the claims of the instant application. Should the Examiner have any further comments or suggestions, the undersigned would very

much welcome a telephone call from him in order to be able to discuss any outstanding issues and to place the application into condition for allowance.

Respectfully Submitted,

Robert W. Becker

Robert W. Becker, Reg. No. 26,255
for applicant(s)

ROBERT W. BECKER & ASSOCIATES
707 Highway 66 East, Suite B
Tijeras, NM 87059

Telephone: (505) 286-3511
Facsimile: (505) 286-3524

RWB:mac

VERSION WITH MARKINGS TO SHOW CHANGES MADE:

IN THE CLAIMS:

43. (Once amended) A method according to claim 28, [wherein a] which includes reducing thermal stressing of a semiconductor wafer [is reduced to a minimum].